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MINNEAPOLIS, MN 55440-1022

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/521,931
Filing Date: July 19, 2005
Appellant(s): THEILER, HELMUT

Tonya S. Drake, Reg. No. 57,861
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed July 6, 2009 appealing from the Office action mailed May 13, 2009.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

WITHDRAWN REJECTIONS

The following grounds of rejection are not presented for review on appeal because they have been withdrawn by the examiner. Claims 6, 9 and 11 are no longer rejected under 35 U.S.C. §102(b) as being anticipated by Peil (US 4,560,909).

The rejection of claims 1-11 and 19-22 under 35 U.S.C. §103(a) as being unpatentable over Dalnodar (US 5,504,400) are maintained.

Claims 2-4, 8-10 and 22 are objected to.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,504,400	Dalnodar	4-1996

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims (the art rejection of Peil has been removed).

Claim Objections

1. Claims 2-4, 8-10 and 22 are objected to because the word "logical" is missing before the recitations of "load control signals" and "detection signals." Consistent terminology must be maintained throughout the claims when referring to the same component or signal. Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-11 and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dalnodar.

With respect to claim 1, Dalnodar discloses a circuit array (fig 4-5; col. 4, line 47 to col. 6, line 37) for controlling operation of two loads (B5, B15) that operate with a rectified AC voltage (1, D5, D15), comprising:

a first current path that includes the first load (top half of 20, including lamp B15 and diode D15);

a second current path that includes the second load (bottom half of 20);

a semiconductor switch (T1) on a circuit path that includes the two loads, the switch being electrically connected to a common node (6) of the first and second current paths; and

a control unit (10, except for triac) to generate a switch control signal (output from diac DC1) that controls the semiconductor switch; wherein the control unit comprises:

a phase detection device (11, 12; col. 5, line 63 to col. 6, line 37) to detect whether a phase of the AC voltage is positive (D11) or negative (D12), and to output a logical detection signal that is based on whether the phase is positive or negative (Vc)(see note A, below); and

a logic unit (diac DC1) to generate the switch control signal (input to T1) based on one or more load control signals (value of potentiometers, VR11-VR12) and the logical detection signal (see note B), wherein the control unit is configured to supply the first current path with a first half wave and to supply the second current path with a second half wave (figs 6a-b; col. 5, lines 34-46).

As discussed above, the limitation of a "logical load control signal" is distinguished from and does not require the presence of a "logic gate."

A: Dalnodar discloses that analog signals are passed from the phase detectors (11,12) to the diac (DC1). Each phase detector (11, 12) only handles one half of the sinusoidal waveform. Accordingly, only one diode (D11, D12) is conducting at any one time. Therefore, the outputs of the diodes are either forward biased or they are not. If the diodes are forward biased, then the diode conducts (HIGH). If the diodes are not forward biased, then the diode does not conduct (LOW). The Dalnodar diodes produce logical 0 or logical 1 outputs based on the voltages present at their inputs, and the input voltages are based on the phase of the voltage source (1). Thus, Dalnodar meets the recited limitation of a phase detection device (11,12) to output a logical detection signal that is "based on" whether the phase is positive or negative.

B: Due to the biasing of the diodes (D11, D12), the variable resistors (VR11, VR12) alternately conduct. During positive half waves, only VR11 is conducting, and during negative half waves, diode D11 prevents current from flowing through VR11 (and vice versa for VR12). Therefore, the voltage drops across VR11 and VR12 and the current through VR11 and VR12 alternate between a relative high and a relative lose.

Thus, Dalnodar meets the recited limitation of "logical load control signals" and that the switch control signal is "based on" one or more logical load control signals and the logical detection signal.

With respect to claim 2, Dalnodar discloses the control unit comprises a time control circuit (VR11-VR12) for generating the load control signals at a predetermined time (col. 5, line 63 to col. 6, line 37). Dalnodar discloses that the selected value of the potentiometers determines the switching time of the triac.

With respect to claim 3, Dalnodar discloses the control unit comprises a sensor circuit (VR11-VR12) for generating the load control signals in response to a sensed condition. Dalnodar discloses the control unit senses the values of the potentiometers and controls the switching time of the triac accordingly.

With respect to claim 4, Dalnodar discloses that the logic unit (diac D1) is only required to process one input at a time (fig 7; col. 6, line 44 to col. 8, line 2). The voltage across the capacitor (Vc) determines the timing of switching the triac (T1). The rate of charge of the capacitor is determined by the potentiometers (VR11-VR12). The interaction-reduction circuit (14) ensures that left over charge from one cycle (positive, for example) does not affect the other (negative cycle).

Dalnodar discloses that both half-cycle charge-rate control circuits (11, 12) share a capacitor (C1) and diac (DC1). At the time of the invention by applicant, it would have been obvious to one skilled in the art to provide a respective capacitor and diac for each of the charge-rate control circuits (11, 12) since it has been held that the mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8 (CCPA 1977). With two inputs to the triac (T1), one skilled in the art would find it necessary to use a multiplexer in order to manage the timing of supplying two controls signals to one triac gate. The multiplexer would ensure that the control signal from the positive wave capacitor is applied only during positive half waves, as vise versa.

With respect to claim 5, Dalnodar discloses the circuit array "is part of" an integrated circuit (figs 4-6).

With respect to claim 6, Dalnodar discloses an electronic device (figs 4-6; col. 4-6), comprising:

an input having leads (4, 5) to receive AC voltage (1);

a circuit array for controlling a switch (T1) to apply voltage to first (B15) and second (B5) loads based on whether a phase of the AC voltage is positive (D11) or negative (D12) and load control signals (VR11-VR12) generated separately for the first and second loads; and

a rectifier (D5, D15) that provides the voltage to the first and second loads, the voltage being generated from the AC voltage (1), wherein the rectifier comprises an open bridge circuit, and wherein the voltage comprises different half waves of the AC voltage, wherein a first half wave is applied to the first load and a second half wave is applied to the second load (col. 3, lines 61-65).

As discussed above, the diodes (D11, D12) are alternatively on (conducting) during positive and negative half waves of the incoming AC cycle. Also, the signals through the diodes and the currents/voltage drops through the resistors alternate HIGH and LOW based on whether the input is positive or negative half wave portion of the complete AC sinusoidal signal. These values meet the amended limitation of "logical" load control and "logical" detection signals.

With respect to claim 7, Dalnodar discloses the phase detection device and logic unit, as discussed above in the rejection of claim 1.

With respect to claims 8-11, Dalnodar discloses the recited limitations, as discussed above in the rejections of claims 2-5, respectively.

With respect to claim 19, Dalnodar discloses that the switch comprises a single triac. At the time of the invention by applicant, it would have been obvious to one skilled in the art to substitute the Dalnodar triac with a MOSFET device, since the two components are art recognized switching devices. Both the triac and MOSFET connect input and output lead lines based on a signal received at their gate.

With respect to claim 20, Dalnodar discloses the circuit array is configured to apply a voltage to the first/second load when a phase of the AC voltage is positive/negative, as discussed above in the rejection of claim 1.

With respect to claim 21, Dalnodar discloses the switch is connected between ground (5) and the two loads (20).

With respect to claim 22, Dalnodar discloses the logical load control signal comprises a logical 0 and a logical 1. As discussed above, only one diode (D11, D12) is conducting at any one time, causing only one resistor (VR11, VR12) to conduct current at a time, thus producing a logical load control signal consisting of a logical 0 and a logical 1.

(10) Response to Argument

Appellant's arguments regarding Peil (Brief, pages 11-15) are moot as the art rejection over Peil has been withdrawn by the Examiner. Beginning on page 15, appellant argues against the §103(a) art rejection in view of Dalnodar.

The Examiner disagrees with the Appellant's interpretation of the switch control signal (Brief, pages 15-16). Claim 1 recites, in part, "a logic unit to generate the switch control signal based on one or more logical load control signals and the logical detection

signal" (emphasis added). The limitation "based on" does not impart structure into the claim. Appellant's argument (Brief, page 16) that the claim calls for the use of two inputs is drawn towards unclaimed subject matter. The Examiner agrees that Dalnodar discloses one input (fig 4, 5b, horizontal line leading into the left side of item DC1). The signal at this input, however, is "based on" several factors, including the value of resistor R1, the values of resistors VR11 and VR12, the orientation of diodes D11 and D12 and the value of capacitor C1. The language of claim 1 does not require a separate input line for each of the logical load control signals and the logical detection signal. The "based on" phrase on claim 1 merely recites that the logical load control and logical detection signals have an effect on the generation of the switch control signal. This limitation is met by Dalnodar.

The Examiner also disagrees with Appellant's interpretation of logical load control signals and logical detection signals. First, the Dalnodar logical load control signal is interpreted as the output of resistors (VR11, VR12). Resistors (VR11, VR12) combine with the resistor (R1) form a voltage divider. The values of the resistors determine the output voltage provided to the diodes (D11, D12) and the biasing of those diodes. The values of the resistors, therefore, control the power provided to the load by controlling the amount of time that the load is energized (Dalnodar; col. 5, line 63 to col. 6, line 27 and lines 27-37). Since the resistors control the brightness of the lamps, the signals output by the resistors meet the limitation of "load control signals."

Second, the Dalnodar logical detection signal is interpreted as the output of the diodes (D11, D12). Only one diode (D11, D12) is forward biased (i.e. "on") at a time

(col. 5, lines 63-64); D11 is positioned such that it can only be "on" during positive half-waves, and D12 is positioned such that is can only be "on" during negative half-waves. If the diodes are "on," then there is a current passing through the diode and the output signal is relatively HIGH (i.e. a logical "1"). If the diodes are "off"," then there is no current passing through the diode and the output signal is relatively LOW (i.e. a logical "0"). Since the biasing of the diodes directly depend on the polarity of the incoming AC wave, the signals output by the diodes meet the broad limitation of being "logical."

While the Examiner agrees that the Dalnodar logical load control signals are analog, there is no requirement in the claims that the logical signals are digital.

The diodes (D11 and D12), as is commonly known with diodes, have a breakdown voltage of about 0.7 volts. If the voltage input to a diode (the "input" to a diode is the anode, also recognizable as the wide base of the sideways triangle forming the diode schematic - the "output" is the cathode shown as a vertical line) is below 0.7 volts, then the output of the diode will be 0 volts. If the voltage input to the diode (D11) is above 0.7 volts (20 volts, for example), then the output of the diode will be the input voltage minus 0.7 volts (i.e. 19.3 volts). Thus, the diodes produce a relative low value (0) and a relative high value (1). The Examiner agrees that this is not digital. The claims, however, do not recite that the signals are digital. The Examiner also agrees that the relative high value provided by the diodes will change (for example, as it increases from 0 to 19.3 in response to the sinusoidal input wave increasing from 0 to 20 volts). The relative high value, however, remains a high value when compared to the low value (0 volts). The claims do not require an absolute voltage level to be

maintained to represent the logical 0 value or the logical 1 value that would be associated with a digital signal. The claims only recite the broader limitation of "logical," which is met by Dalnodar.

Appellant then repeats an old interpretation of the reference made by the Examiner (Brief, bottom of page 17 and page 18). This interpretation, however, was withdrawn in the most recent Office Action (Final Rejection, May 13, 2009). The Examiner's arguments presented in November, 2008 are not germane to the appeal at hand, as this interpretation is no longer relied upon.

Appellant rebuts the new interpretation made by the Examiner (Brief, top of page 19) by stating that "the signal provided to the diac DC1, is not a logical signal, but is rather the analog signal provided by capacitor C1." The Examiner agrees that the signal provided to the capacitor is analog. The claims, however, do not recite that the signal is not analog. The broad limitation of "logical" is not equivalent to "digital." The limitation recited in the claim is met by Dalnodar. Appellant has not provided any other arguments or support for this argument, except to infer that analog is not logical.

Regarding claim 6, Appellant argues that the Dalnodar signal is analog (Brief, middle of page 19). As discussed above, the Examiner agrees with this statement. The claims, however, do no recite that the signal is not analog.

The Examiner disagrees with Appellant's argument that Dalnodar fails to meet the limitation that the logical load control signals are generated separately for the first and second loads (Brief, bottom of page 19). The Examiner agrees with Appellant's statement that Vc is positive at the end of a positive cycle and Vc is negative at the end

of a negative cycle (Brief, page 20, first paragraph). These values are the two signals, as will be expanded upon below.

Dalnodar disclose that during positive half waves, power flows through the positive half-cycle charge-rate control circuit (11) and the value of the resistor (VR11) controls the charging of capacitor (C1)(Dalnodar, col. 5, lines 63-67). The value of capacitor (C1) determines if the diac (DC1) breaks down which then causes the triac (T1) to switch (col. 6, lines 1-12). Also during the positive half-waves, only the first current path (B15, D15) is on (col. 6, lines 13-27). Thus, the value of resistor (VR11) determines the brightness of bulb (B15). Similarly, resistor (VR12) determines the brightness of bulb (B5)(col. 6, lines 28-37). Thus, load control signals are "generated separately for the first and second loads." Further, the reference explicitly discloses that "adjustment of either potentiometer VR11 or VR12 should control the selected channel but should not affect the other channel" (col. 6, lines 44-47; emphasis added).

The Examiner agrees that the Dalnodar "logical load control signals" are provided to the diac (DC1) on the same input line (fig 4, 5b; horizontal line connecting the + node of C1 to the left side of the diac DC1). Claim 6, however, recites "a circuit array for controlling a switch to apply voltage to first and second loads based on whether a phase of the AC voltage is positive or negative and logical load control signals generated separately for the first and second loads" (emphasis added). As discussed above, the limitation of "based on" does not impart structure into the claim and does not require separate input lines. Dalnodar discloses that the logical load control signals are generated separately (in item VR11 during positive half-waves; in item VR1212 during

negative half-waves; see col. 6, lines 44-47). Dalnodar also discloses that the switch control signal is "based on" the phase of the AC voltage (determined by D11, D12) and the logical load control signals (determined by VR11 and VR12).

Regarding claim 7 (Brief, top of page 21), it is noted that the claim depends from claim 6, not claim 1. As discussed above, the limitation of "logical" does not require digital and "logical" does not discount an analog signal that is passed through a diode to result in relative low (0) and relative high (1) voltage values.

Regarding claim 19, the Examiner agrees with the general description of the Dalnodar triac (T1) and the claimed MOSFET. The Examiner, however, disagrees with appellant's conclusion regarding the use of the individual devices. Appellant argues that because the Dalnodar triac can be triggered with two voltages, it cannot be substituted with a MOSFET (triggered by one voltage). The Examiner disagrees with this argument.

Although the triac is a bidirectional electronic switch, Dalnodar still uses the switch to:

1) complete or block the current path for each load; and

2) control the amount of time the current path is completed, and thereby controlling the amount of power provided to the loads.

The difference in Appellant's MOSFET (fig 2, item 14) and Dalnodar's triac (fig 4, item T1) is only based on configuration of the system. In appellant's design, the switch (14) turns on or off to complete a current path for each load. The polarity of the input power is independent of the status of the switch (setting aside the phase detection

device for the moment). What this means is an off switch has the same effect on the system regardless of if the input power is positive or negative. This is because all power flow (positive and negative half-waves) in Appellant's figure 2 is clockwise. In Dalnodar's design, the switch changes between forward-biased and reverse-biased. The polarity of the input power is directly related to the status of the switch (setting aside the components of item 9). What this means is an off switch during a positive half-wave automatically becomes an on switch during a negative half-wave because current is now flowing in the opposite direction due to the orientation of the figure and the placement of the rectifier (D5, D15). This is because the positive half-wave power flow is clockwise and negative half-wave power flow is counter-clockwise.

The Dalnodar switch (T1) meets every limitation presented in the pending claims regarding the position of the switch and control of the switch depending on a phase detection signal and one or more load control signals. The substitution of a MOSFET for a triac in the system would be obvious to one skilled in the art, since the two components are art recognized equivalents switching devices. Substituting one component for the other requires only minor modifications to the circuitry to compensate for the known bidirectional conduction properties of the triac. Such modification is well within the level of ordinary skill in the art, through calculation or minor trial and error.

Regarding claim 21 (Brief, page 23), "ground" is commonly referred to in electric circuitry as the lowest potential of the system. It is a reference point from which to measure the voltage present at all other parts of the circuit. During positive half-waves, conductor 5 experiences the lowest-potential as compared to the rest of the current path

(4, 6, S1, 5). This is because the power output by source (1) has passed through several components (B15, B5, 6, T1, S1 and 5). The selection of a reference point (i.e. ground) has no impact on the rest of the system. Thus, conductor 5 can be viewed as the reference point known as "ground." Similar interpretations are made for conductor 4 during negative half-waves.

Regarding claim 22 (Brief, top of page 24), as discussed above, the Dalnodar diodes (D11, D12) are either biased (1) or they are not (0). A signal can be analog and still be a relative high (1) or a relative low (0) signal. There is no requirement in claim 22 that the signal is digital.

Regarding the objections to claims 2-4, 8-10 and 22, Appellant amended the independent claims (October 22, 2008) to add the limitation that the load control signals and the detection signal are "logical." The dependent claims listed above, however, were not similarly amended. The Examiner made this objection because consistent claim language must be maintained when referring to the same component or limitation.

Claims 1-11 and 19-22 are not allowable for the reasons provided above. Dalnodar discloses the switch control signal is "based on" several factors, including the phase of the input signal (logical detection signal) and logical load control signals (their source or meaning is undefined in the claims). Dalnodar also discloses the detection signal and the load control signals are "logical."

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Adi Amrany /Adi Amrany/
Examiner, Art Unit 2836

Conferees:
/Stephone B. Allen/
Supervisory Patent Examiner, Art Unit 2872

/Rexford N BARNIE/
Supervisory Patent Examiner, Art Unit 2819